REMARKS

The above amendments and following remarks are submitted in response to the Official Action (i.e., Paper No. 12) of the Examiner mailed December 22, 2003. Having addressed all objections and grounds of rejection, claims 1-25, being all the pending claims, are now deemed in condition for allowance. Entry of this amendment and reconsideration to that end is respectfully requested.

The Examiner rejected claim 1 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. In response thereto, claim 1 has been amended in accordance with the suggestion of the Examiner.

Claims 11 and 16[1] have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,850,534, issued to Kranich (hereinafter referred to as "Kranich"). In response thereto, claims 11 and 16 have been amended. Specifically, claim 11 has been amended to require dedicated paths for data and tag storage within the level two cache memory and routing of the SNOOP request via the dedicated tag storage access path. Similarly, claim 16 has been amended to also require separate

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[1]Though paragraph 7 of Paper No. 12 refers to claim "18", it is assumed that this is a typographical error, and claim "16" is deemed rejected as anticipated by Kranich.

paths between the system bus and each of the data and tag stores of the level two cache memory.

These amendments are deemed to clearly distinguish over Kranich, because the Examiner admits at paragraph 9 of Paper 12:

> However, Kranich does not specifically teach the improvement comprising a first dedicated path between said system bus and said cache storage and a second dedicated path between said system bus and said tag storage as recited in the claim.

Thus, claims 11 and 16, as amended, and all claims depending therefrom, are deemed allowable over the current rejection of record.

Claims 1, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of U.S. Patent No. 6,247,094, issued to Kumar et al (hereinafter referred to as "Kumar"). This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as specified by MPEP 2143.

A key requirement of MPEP 2143 is that the alleged combination (i.e., Kranich in view of Kumar in this case) must contain all of the claimed limitations. Each of these claims requires a dedicated path from the system bus to the level two cache tag storage which is separate from the path from the system bus to the level two cache data storage. The importance of this feature is found in Applicants' specification in numerous places including page 7, lines 13-18.

The Examiner admits that Kranich does not have this feature. However, he clearly erroneously states:

> Kumar discloses a data processing system for reducing cache latency wherein the improvement comprises a first dedicated path between a system bus and a cache storage [front side bus 190 communicates with L2 data array by means of line connected to way predictor 150; Fig. 7], and a second dedicated path between a system bus and a tag storage [front side bus 190 communicates with L2 tag array 135 by means of snoop queue line; Fig. 7]....

This statement is clearly erroneous because both L2 Tag Array 135 and L2 Data Array 120 communicate with Front Side Bus 190 via Bus Controller 130. This is in stark contrast to Applicants' claimed invention explained at page 14, lines 8-10, which states:

> Unlike prior art system controller[s], bus interface logic 60 provides separate and independent paths to ....

Though the Examiner has not presented the required evidence of "motivation" and "reasonable likelihood of success", the lack of all claim elements in the alleged combination is the most apparent. The rejection of claims 1, and 6-7, and all claims depending therefrom, is respectfully traversed.

Claims 2 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Kumar and further in view of U.S. Patent No. 5,426,765, issued to Stevens et al (hereinafter referred to as "Stevens"). The ground of rejection is respectfully traversed for the following reasons.

Claim 2, for example, depends from claim 1 and is further limited by "control logic directly coupled to said cache storage

and said tag storage which provides the highest priority for said SNOOPing". In ignoring the actual claim limitation, the Examiner states:

> Stevens discloses a control logic which provides the highest priority for a SNOOPing [col. 4, lines 23-32].

A cursory comparison between this finding and the actual claim limitation readily shows that even if the Examiner's finding were correct, it is insufficient to meet the claimed invention. The rejection of claims 2 and 8 is respectfully traversed.

Claims 3-5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Kumar and further in view of Stevens and further in view of U.S. Patent No. 6,353,877, issued to Duncan et al (hereinafter referred to as "Duncan"). This ground of rejection is respectfully traversed for the following reasons.

With regard to claim 3, for example, the Examiner again refuses to consider the actual claim limitation. He states:

> Duncan discloses a multiprocessing system comprising a duplicate tag store [col. 7, lines 30],....

However, the claim is limited to a specific location for the duplicate tag store. It is not just thrown into the system anywhere. Claim 3 actually reads: "wherein said level two cache memory further comprises a duplicate tag memory". The claimed invention requires the duplicate tag memory to be a part of the level two cache memory. This is necessary to practice

Applicants' invention. A cursory review of Fig. 2 of Duncan shows that Duplicate Tag Store 54 is not located within or a part of Secondary Cache 48. The rejection of claims 3-5 is respectfully traversed.

Claim 9 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Kumar in view of Stevens and further in view of U.S. Patent No. 6,457,087, issued to Fu (hereinafter referred to as "Fu"). This ground of rejection is respectfully traversed for the following reasons.

In supporting his rejection, the Examiner clearly erroneously states:

> Fu discloses a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within a level one tag memory (i.e., L2 duplicate tag memory 234) [Fig. 5A]. (emphasis added)

This finding is clearly erroneous because it is inconsistent with Fu, which states at column 7, lines 56-59:

> The duplicate L2 tag memory 234 contains a set of duplicate cache tags, one for each data block in the processor's L2 cache memory 222. (emphasis added)

Thus, Fu's duplicate tag memory 234 keeps duplicates of L2 cache memory tags rather than Level one cache memory tags as claimed. The rejection of claim 9 is respectfully traversed as based upon a clearly erroneous finding of fact.

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Kumar in view of Stevens in

view of Fu and further in view of Duncan. This ground of rejection is respectfully traversed.

In making his rejection, the Examiner alleges a five reference combination which is almost incredible on its face. Nevertheless, the most important thing is that the Examiner again ignores the specific claim limitation which reads: "wherein said SNOOP request is directly coupled to said duplicate tag memory". After alleging the combination of five references, there is still no showing of direct coupling of the SNOOP request to the duplicate tag memory. Instead the Examiner cites Duncan, column 8, lines 11-13, which states:

> All devices that are coupled to system bus 20, at step 72 monitor this bus transaction by snooping the bus and present the address to heir duplicate tag store...

The citation specifically shows the lack of "direct coupling". The rejection of claim 10 is respectfully traversed.

Claims 12 and 17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens. This ground of rejection is respectfully traversed for the reasons provided above with regard to the discussions of claim 2.

Claim 13 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens and further in view of Fu. This rejection is respectfully

traversed for the reasons provided above with regard to the rejection of claim 9.

Claims 14 and 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens in view of Fu and further in view of Duncan. This ground of rejection is respectfully traversed for the reasons provided above with regard to claim 10.

Claim 18 has been rejected as under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens and further in view of Kumar. This ground rejection for the reasons discussed above with regard to claim 10.

Claim 19 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens in view of Kumar and further in view of Fu. As explained above with regard to claim 9, Fu's L2 duplicate tag memory 234 duplicates L2 rather the level one cache memory tags. The rejection of claim 19 is respectfully traversed.

Claim 20 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens in view of Kumar in view of Fu and further in view of Duncan. As explained above, this alleged combination of five references has a number of pieces. However, it does not have the claimed "direct coupling" and in fact teaches against it.

Newly presented claims 21-25, though differing in scope from previously pending claims 1-20, are deemed allowable for similar reasons. Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-25, being the only pending claims.

Respectfully submitted,

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By their attorney,

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